HARDWARE

REFERENCE DESIGN

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UC6580x-00

Dual-frequency GNSS Positioning Chip

Revision History

Version	Revision History	Date
R1.0	First release	Sep., 2023
R1.1	Update the design related with V_BACK Update the description of RTC in section 2.3 Update the model to UC6580x-00 by adding the sub-model	Mar., 2024
R1.2	Update the description of VBCKP in section 2.1	Mar., 2024

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Foreword

This document gives the hardware reference design of the chip UC6580x-00 from Unicore.

Target Readers

This document applies to technicians who possess the expertise on GNSS receivers.

Contents

1 Reference Design

> ☞ If you do not need the RTC and backup function, connect V_BACK to VDD_IO.

RTC and backup function are the prerequisites of GNSS hot start. Refer to *UC6580x-00 Datasheet* for more details.

1.1 LDO Mode

Under the LDO mode:

- DCDC_IN and VDD_IO use the same power supply;
- Use the internal LDO_EX to power the system;
- Power the external TCXO by LDO_X;
- Connect RTC Crystal externally;
- Connect LNA and SAW externally;
- Use the UART interfaces to communicate;
- Lower cost but higher power consumption.

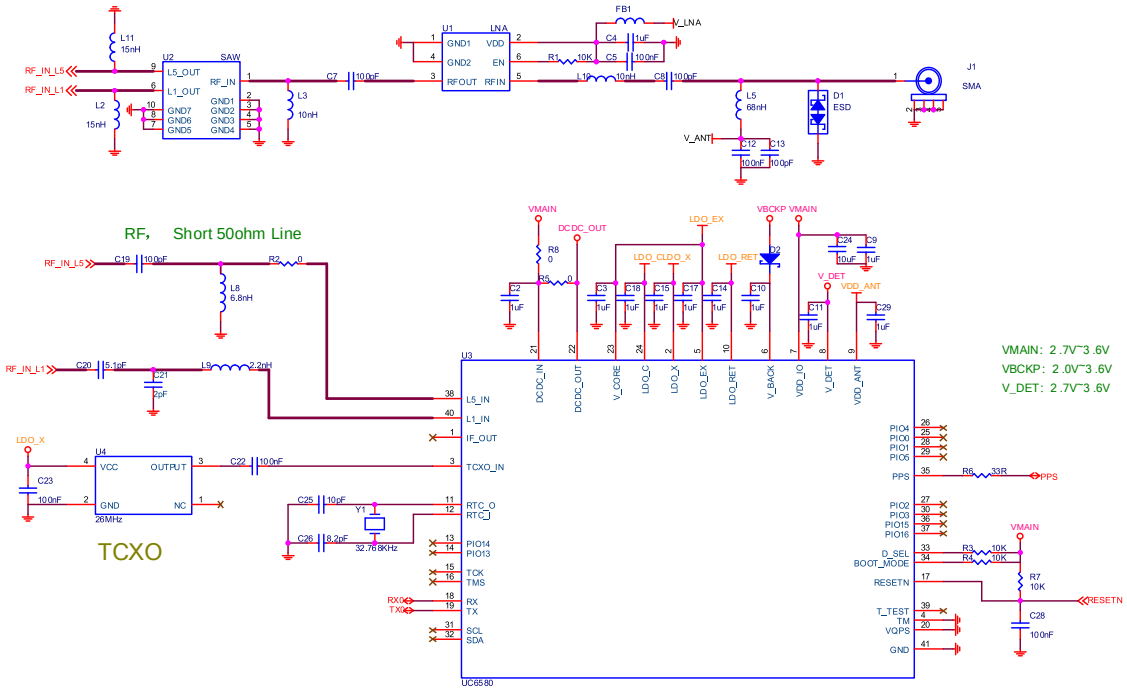


Figure 1-1 Reference design of LDO mode

> ☞ If the antenna feed supply and the chip's main supply use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on the main supply, which may cause damage to the chip. Therefore, it is recommended to design an independent power rail for the antenna feed supply to reduce the possibility of chip damage.

1.2 DC/DC Mode

Under the DC/DC mode:

- DCDC_IN and VDD_IO use the same power supply;
- Use the internal DC/DC to power the system;
- Power the external TCXO by LDO_X;
- Connect RTC Crystal externally;
- Connect LNA and SAW externally;
- Use the UART interfaces to communicate;
- Lower power consumption but higher cost due to the use of power inductor comparing with LDO mode;

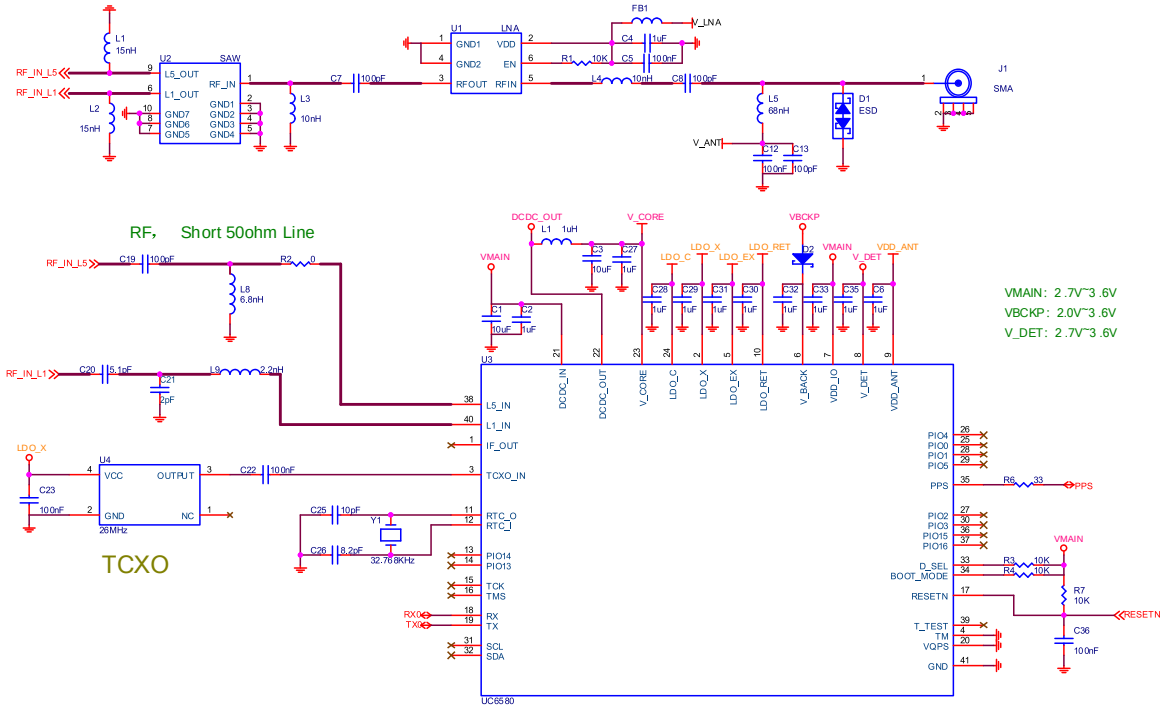


Figure 1-2 Reference design of DCDC mode

If the antenna feed supply and the chip's main supply use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on the main supply, which may cause damage to the chip. Therefore, it is recommended to design an independent power rail for the antenna feed supply to reduce the possibility of chip damage.

2 Attention

2.1 Power

DCDC_IN and VDD_IO use the same external power supply. For all the power supplies, the ripple voltages must not exceed 50 mV.

The value of LDO_X must be lower than VDD_IO and the default is 1.7 V to 1.9 V.

To improve the product stability, it is recommended to control the power on and off of UC6580x-00 by the controlling terminal of the power supply. When an unstable factor out of control occurs, the terminal does power on/off operations on UC6580x-00 to make the system recover, which ensures a continuous work of the system.

Note:

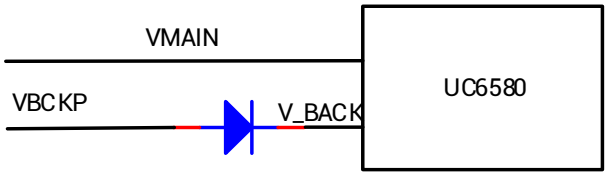
VMAIN

- The VMAIN initial level when power-on should be less than 0.4 V.
- The VMAIN ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VMAIN.
- VMAIN power-on waveform: The time interval from 10% rising to 90% must be within 100 µs ~ 10 ms.
- Power-on time interval: The time interval between the power-off (VMAIN < 0.4 V) to the next power-on must be larger than 500 ms.

VBCKP

- The VBCKP initial level when power-on should be less than 0.4 V.
- The VBCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VBCKP.
- VBCKP power-on waveform: The time interval from 10% rising to 90% must be within 100 µs ~ 10 ms.
- Power-on time interval: The time interval between the power-off (VBCKP< 0.4 V) to the next power-on must be larger than 500 ms.
- To prevent a reversed current from VMAIN to V_BACK, the supply voltage of V_BACK should be no lower than VMAIN (not considering the problem of voltage reduction when the backup battery is short of power) or you should add a forward biased diode before V_BACK. Meanwhile, make sure that the voltage of V_BACK is within the range of 1.7 V to 3.6 V. The diode is recommended to be of low power (mA-level

forward current), low forward voltage drop (300 mV), and low reverse leakage current (< 100 μA within the working temperature).



2.2 Reset Signal

UC6580x-00 supports system reset. The reset signal is active low and the active time should be no less than 5 ms.

2.3 RTC

RTC is usually driven by an on-chip 32.768 kHz oscillator, which needs to be connected to an external 32.768 kHz crystal. It supports three kinds of connections:

1) Use an external crystal, as the schematic diagrams show.
2) Use an external 32.768 kHz digital clock signal to directly input to RTC_I, and it is recommended to do ESD protection at the RTC_I pin. Make sure that the signal amplitude is less than 1.98 V, otherwise it may cause damage to the chip. Keep RTC_O floating.
3) When RTC is not used, keep RTC_I floating and connect RTC_O to Ground to reduce the current leakage.

In addition to the general rules of RTC layout and routing, you should pay special attentions to:

- Have a complete reference GND under the chip and the RTC crystal.
- The RTC crystal shall be placed as close to the chip as possible, and there shall be no other devices between the two;
- Devices, signals, wiring, etc. with high power or strong interference should be avoided around RTC crystal;
- It is recommended to do ground shields for the relevant circuits of RTC.

2.4 TCXO

The CLK_I pin connects an external TCXO of 26 MHz. The power supply of TCXO can be LDO_X or an external independent LDO power supply.

In order to ensure the chip boots normally, the 26 MHz clock should work stably no later than 10 ms after the chip is powered.

The basic parameter requirements for TCXO are as follows:

- Frequency and temperature: 26 MHz ± 0.5 ppm (-40 °C to +85 °C);
- Short-term frequency stability: < 5 ppb/s.

Special attentions should be paid to the layout and routing of TCXO in addition to the general rules:

- It is recommended to maintain copper void for the layer where TCXO is placed and the adjacent layers, and keep the reference ground complete for other layers, so as to reduce the impact of heat conduction on the performance of TCXO.
- Place TCXO as close to the chip as possible, with ground shields for the surrounding circuits.
- Avoid placing any high-power or strong interference devices, signals, traces, etc. around the TCXO. Keep a distance of more than 3 times the trace width between the clock signal trace and other traces.

3 Recommended BOM

Table 3-1 Recommended BOM

Category	Description	Type	Manufacturer
Capacitor	0402 surface mount capacitor 10 μF, ±20%, X5R, 6.3 V	CC0402MRX5R5BB106	YAGEO
Capacitor	0201 surface mount capacitor 1 μF, ±20%, X6S, 6.3 V	GRM033C80J105ME05D	Murata
Capacitor	0201 surface mount capacitor 100 nF, ±10%, X7S, 10 V	C0603X7S1A104K030BC	TDK
Capacitor	0201 surface mount capacitor 100 pF, ±10%, X7R, 25 V	CC0201KRX7R8BB101	YAGEO
Capacitor	0201 surface mount capacitor 10 pF, ±2%, COG, 50 V	GRM0335C1H100GA01D	Murata
TVS	ESD protective diode DFN0603-2L 1100 W ±18 kV	JEB05UCDS-AH	JIEJIE MICROELECTRONICS CO. , Ltd
Ferrite Bead	Ferrite Bead BLM15AG221SN1D	BLM15AG221SN1D	Murata
Inductor	Chip inductor: 1 μH DC resistor: 300 mΩ Maximum current: 0.7A Tolerance: ±20% Size: 1.6 mm × 0.8 mm × 0.95 mm	MLP1608V1R0BT0S1	TDK
Resistor	Surface Mount 0 Ω, 1/16 W, ±5%, 0402	RC0402JR-070RL	YAGEO
Resistor	Chip resistor 0 Ω, 1/20W, ±1%, 0201	RC0201FR-070RL	YAGEO
Resistor	Chip resistor 10 kΩ, 1/16 W, ±5%, 0402	RC0402JR-0710KL	YAGEO
Resistor	Chip resistor 10 kΩ, 1/20 W, ±1%, 0201	RC0201FR-0710KL	YAGEO
Resistor	Chip resistor 4.7 kΩ, 1/16 W, ±5%, 0402	RC0402JR-074K7L	YAGEO

Category	Description	Type	Manufacturer
Resistor	Chip resistor 4.7 kΩ, 1/20 W, ±5%, 0201	AC0201JR-074K7L	YAGEO
Resistor	Chip resistor 33 Ω, 1/16 W, ±5%, 0402	RC0402JR-0733RL	YAGEO
LNA	High gain, dual-band LNA LGA 6-pin	MXDLN14TP	MAXSCEND
SAW	1.5 mm × 1.1 mm 1166 MHz to 1187 MHz 1559 MHz to 1606 MHz L1: 2.4 dB Max. L5: 2.0 dB Max. L1: 50 MHz L5: 20 MHz	MXDFD14A1	MAXSCEND
TCXO	±0.5 ppm 26 MHz 2.0 mm × 1.6 mm × 0.73 mm	X1G005441020416	EPSON
Crystal	32.768 KHz ±20 ppm -40 °C to +85 °C	1TJG125DR1A0004	KDS
Crystal	32.768 KHz ±20 ppm 12.5 pF -40 °C to +85 °C	X1A000061000200	EPSON

Appendix Simplest Design to Replace UC6226

UC6580x-00 can replace the UC6226 (QFN40) in the circuits. If your product uses UC6226 (QFN40), you can upgrade it with UC6580x-00. Please contact Unicore FAE if necessary.

This section introduces the simplest way to fulfill the replacement. You can design your circuits according to Figure 0-1 and Table 0-1. Make sure that DCDC_IN and VDD_IO use the same power supply and note that you need to adjust the value of the DCDC output inductor (L2), RF_IN matching inductor (L3) and RF_IN matching capacitor (C14).

Except the pins listed in Table 0-1, the other pins of the UC6580x-00 (QFN40) and UC6226 (QFN40) are the same.

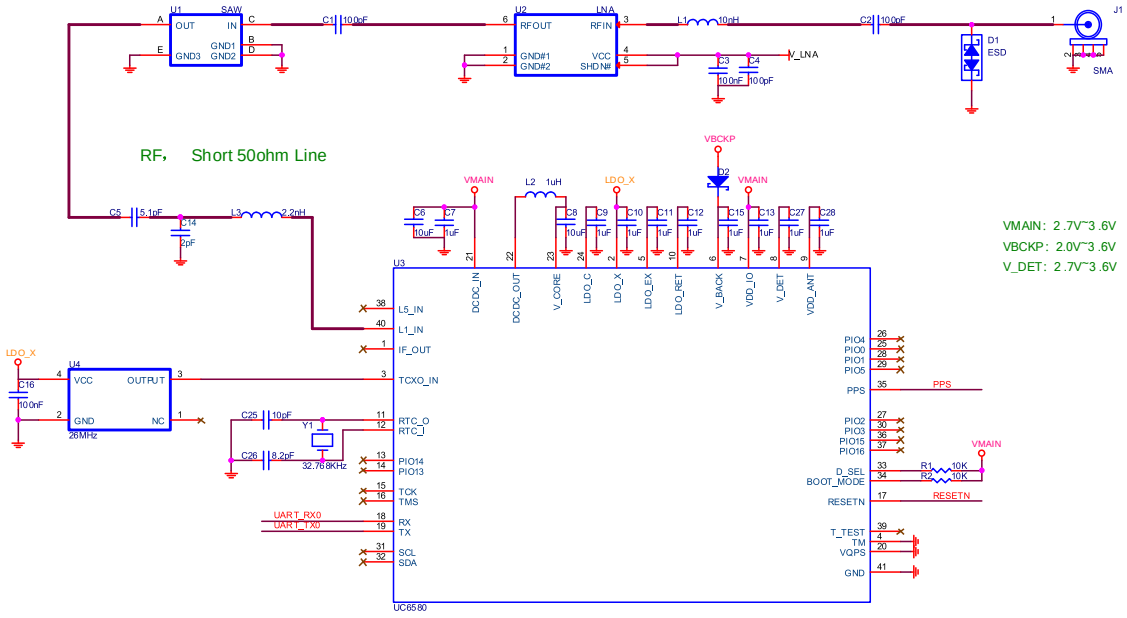


Figure 0-1 Simplest design to replace UC6226

Table 0-1 Simplest design to replace UC6226

Pin No.	UC6226NI/AS	UC6580x-00	Description
1	VDD_ANA	IF_OUT	UC6580x-00: floating Not compatible
4	XTAL_O	TM	Both floating Compatible
5	LDO_F_OUT	LDO_EX	Both connect a 1 μF capacitor externally Compatible
8	PIO17	V_DET	UC6580x-00: can be floating or connect a 1 μF capacitor externally Partially compatible
9	NC	VDD_ANT	UC6580x-00: can be floating or connect a 1 μF capacitor externally Partially compatible
10	PIO18	LDO_RET	UC6580x-00: connects a 1 μF capacitor externally Not compatible
20	T_SENSE	GND	UC6580x-00: connects Ground Not compatible
22	V_DCDC_OUT	DCDC_OUT	UC6580x-00: L2 = 1μH, C8 = 10 μF Not compatible
38	LDO_RF_OUT	L5_IN	UC6580x-00: connects RF signals if L5 channel is used, otherwise floating Not compatible
39	VDD_LNA	T_TEST	UC6580x-00: internal test pin, floating Not compatible
40	LNA_IN	L1_IN	UC6580x-00: L3 = 2.2 nH, C14 = 2.0 PF Not compatible

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